## The I/O Hardware Limitation of NY8 ICE

Description: There are two kinds of I/O hardware limitations for NY8_ICE, which should be taken care of during emulation. These issues were only existed on NY8_ICE and have no relationship between NY8_ICE and real NY8 OTP IC. We strongly suggest customers doing evaluation again on NY8 OTP IC after development.

Reason: 1. FPGA Differential I/O Pin Pair

1) NY8_ICE is based on Xilinx FPGA, the FPGA pins were designed compatible for differential pin pair originally. The FPGA equivalent circuit diagram is shown as following diagram. In this case, there will be potential issue when two nearly pins are used as input pins for data or interrupts. One of input pin will possibly effect to the other if they are differential pair pins as shown in next page.


Figure 12: Potential Design Failure Scenario
(Extract from Xilinx datasheet)
2) Differential I/O Pin Pair Mapping to NY8_ICE IO Port

| Xilinx differential pin pair | P | N |
| :---: | :---: | :---: |
| 1 | - | PAO |
| 2 | PA1 | PA2 |
| 3 | PA3 | - |
| 4 | PA4 | PA5 |
| 5 | PA6 | PA7 |
| 6 | PB0 | PB1 |
| 7 | PB2 | PB3 |
| 8 | PB4 | PB5 |
| 9 | PB6 | PB7 |
| 10 | PC0 | PC1 |
| 11 | PC2 | PC3 |
| 12 | PC4 | PC5 |
| 13 | PC6 | PC7 |
| 14 | PD0 | PD1 |
| 15 | PD2 | PD3 |
| 16 | PD4 | PD5 |
| 17 | PD6 | PD7 |
| 18 | PE0 | PE1 |
| 19 | PE2 | PE3 |
| 20 | PE4 | PE5 |
| 21 | PE6 | PE7 |

3) Example

Wake-up pin is PB0, if users trigger the PB1 it could wake up IC.
2. FPGA Pull-High / Pull-Low Resistors

1) NY8_ICE uses FPGA to emulate IC, however the design of FPGA cannot configure internal pull-high / pull-low resistors on the pins. Instead, external resistors on PCB are used. The users should be aware that, there is 10us pull-up resistor raise time before NY8_ICE IO is pulled to a high level (RC charge time). It should wait until then and entering Sleep/Standby mode, otherwise there are chances that it will not enter Sleep/Standby mode. The reason of this is that the pin has not reach to the logical level " 1 ", and will get to level high after sleep, thus IC is wakened up. The users should also aware of the delay time of IO state transition, including reading IO status.
2) This issue can be solved by setting IO to Output High and then changing it to Input Pull-High, and there will be no need for waiting.
3) Program Example

For example, Pull-High time is about 10 us, if MCU running at $20 \mathrm{MHz} / 2 \mathrm{~T}$ will take 10 system clocks to reach level high.


